UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/486,779	03/02/2000	ALEX Q. HUANG	01640052AA	2967

30743 7590 05/06/2004

WHITHAM, CURTIS & CHRISTOFFERSON, P.C.
11491 SUNSET HILLS ROAD
SUITE 340
RESTON, VA 20190

EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/486,779	HUANG, ALEX Q.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- Th MAILING DATE of this communication appears on the cov r she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,19-32,38,45 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-22 and 46* is/are allowed.

6)☒ Claim(s) *1-9,23-32,38 and 45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The drawings are objected to because fig. 3A of the formal drawing filed on 2/26/04 does not match with the drawing correction of fig. 3A filed on 8/22/03. In addition, figs. 14A, 14B, 17B of the formal drawing filed on 2/26/04 do not match with drawing corrections of figs. 14A, 14B, and 17B filed on 8/23/02. In the formal drawing of fig. 14A, it is unclear why the circuit diagram of the PMOS [236] in fig. 14A is different from the circuit diagram of the PMOS [236] in fig. 14B. What are the shaded rectangle and the shaded triangle in the left side of fig. 18? What are the shaded triangle and the symbol "B" in the left side of fig. 19? A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Claims 23, 32 and 38 are objected to because of the following informalities: Claim 23, lines 20-21, the phrase "said GTO device package" has no antecedent basis. Claim 32, line 7, the phrase "said gate" has no antecedent basis. Claim 38, lines 6, 7, 10 and 11, the phrase "said thyristor device" has no antecedent basis. Appropriate correction is required.

3. Claims 1-9, 26, 31, 32, 38 and 45 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification never discloses a thyristor device package comprising means for injecting current into said thyristor gate for triggering said thyristor into a latching state

and a first voltage applied to a gate terminal of said first MOS transistor causes a forward current to flow between said cathode terminal and said anode terminal turning said thyristor device package to an on state as claimed in claim 1.

Figs. 17A to 17D show an ETO thyristor device package having a thyristor [400], a first plurality of discrete transistors Q1 and a second plurality of discrete transistors Q2. The specification never discloses a thyristor device package comprises the claimed structures as claimed in claims 2-4 and 6-9.

Figs. 17A to 17D disclose the first MOS transistor Q1 comprises a NMOS transistor. The specification never discloses the first MOS transistor comprises a PMOS transistor as claimed in claim 5.

The specification never discloses the MOS transistors of the second plurality of discrete switching devices having respective gates connected to the gate terminal of the first discrete switching device as claimed in claim 26.

Fig. 18 discloses a first feedback path [500] connecting a gate terminal G of a first discrete switching device Q1 to an emitter of a thyristor [502] and a second feedback loop connecting the gate terminal G of the first discrete switching device Q1 to a gate of the thyristor. The specification never discloses a first feedback path connecting said gate of said MOS transistors (the second plurality of discrete switching devices (claim 26)) to said thyristor emitter, and a second feedback path connecting said gate of said MOS transistors (the second plurality of discrete switching devices (claim 26)) to said thyristor gate through a diode as claimed in claim 31.

Fig. 19 discloses a capacitor [C600] connected in parallel to the second discrete switching device Q2. The specification never discloses a capacitor connected in parallel to said MOS transistor (the first discrete switching device (lines 3-5 of claim 32)) connecting said second terminal of said MOS transistor to said thyristor gate as claimed 32.

The specification never discloses a thyristor device package including means for injecting current into the thyristor gate for triggering the thyristor into a latching state as claimed in claim 38.

4. Claims 23-32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23, lines 8-9, the phrase "a first terminal of said first plurality of discrete switching devices" is unclear whether it is being referred to "a first terminal of each of said first plurality of discrete switching devices"; lines 10-12, the phrase "a second terminal of said first plurality of discrete switching devices" is unclear whether it is being referred to "a second terminal of each of said first plurality of discrete switching devices"; lines 16-17, the phrase "a first terminal of said second plurality of discrete switching devices" is unclear whether it is being referred to "a first terminal of each of said second plurality of discrete switching devices"; lines 18-19, the phrase "a second terminal of said second plurality of discrete switching devices" is unclear whether it is being referred to "a second terminal of each of said second plurality of discrete switching devices".

Claims 26-30, lines 2-4, the phrase "said discrete switching devices of said second plurality of discrete switching devices" is unclear whether it is being referred to "said second plurality of discrete switching devices".

Claim 32, lines 3-4, the phrase "said discrete switching devices of said first plurality of discrete switching device" is unclear whether it is being referred to "said first plurality of discrete switching devices".

5. Applicant's arguments filed 2/26/04 have been fully considered but they are not persuasive.

It is urged, in page 13 of the remarks, that the inclusion of a floating ohmic contact, metal strap and the like in an ECT device are literally and explicitly illustrated and described and corresponding electrical nodes and structures are also illustrated and described in connection with hybrid (e.g. ETO) devices and device packages. However, the floating ohmic contact, metal strap and the like in an ECT device are parts of the integrated structures of an ECT device. They are different from the discrete structures of the ETO device package in figs. 17A to 17D. The ETO device package only comprises first and second discrete MOS transistors formed separately from a thyristor device. There is no floating ohmic contact, metal strap and the like in the ETO device package.

6. Claims 19-22 and 46 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
May 4, 2004

Steven Loke
Primary Examiner